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		STA	TEMENT UNI	DER 37 CF	R 3.73(t	Atty. Docket No. 3222.1970004				
Applicant/Patent Owner: Garg et al.										
		6,044,4			ssue Date	e: March 28, 2000				
Titled:	RISC MICROPROCESSOR ARCHITECTURE IMPLEMENTING MULTIPLE TYPED REGISTER SETS									
Intellectual Venture Funding LLC , a Limited Liability Company (Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.										
states that it is:										
1. X	the assignee of	f the entire right, title, and	I interest in;							
2.	an assignee of less than the entire right, title, and interest in (The extent (by percentage) of its ownership interest is%); or									
3.	the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)									
the paten	the patent application/patent identified above, by virtue of either:									
A	An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel, Frame, or for which a copy therefore is attached.									
OR										
В. Х						above, to the current assignee as follows:				
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		S-MOS Syste				Seiko Epson Corporation				
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X	Additional doc	uments in the chain of titl	e are listed on :	a supplemen	tal sheet	(s).				
As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.										
[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]										
The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.										
S	Signature	711. 411.		_		Date				
Dor	nald J. Feathers	stone, Registration N	o. 33,876			Authorized Person				
Printed or Typed Name Title										

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

## Statement Under 37 CFR 3.73(b) (PTO/SB/96) Supplemental Sheet for Chain of Title, Item B

Applic	cant/Owner:	Garg et al.									
Applic	cation No./Pat	ent No.:	6,044,449								
Applic	cation Date/Iss	sue Date:	March 28, 2000								
Title: RISC MICROPROCESSOR ARCHITECTURE IMPLEMENTING MULTIPLE TYPED REGISTER SETS											
Name	of Assignee: Intellectual Venture Funding LLC										
Туре	of Assignee:	Limited	Liability Company	y							
Part B	Continued: A	dditional D	ocuments in the Ch	ain of Title							
4.	From:	Transr	neta Corporation	To:	Transmeta LLC						
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